REMARKS

Applicants thank the Examiner for acknowledging receipt of Applicants' foreign priority document pursuant to 35 U.S.C. §119.

Applicants have also submitted concurrently herewith a proposed Drawing Amendment which modifies Figures 4B and 6-11 as requested by the Examiner. Applicants request entry of these proposed drawing modifications.

Applicants respectfully request reconsideration of the prior art rejection set forth by the Examiner under 35 U.S.C. §§ 102 and 103. Applicants respectfully submit that the prior art references of record whether considered alone, or in combination, fail to either teach or suggest Applicants' presently claimed invention.

Applicants' claimed invention is directed to new and improved techniques for manufacturing semiconductor devices. More specifically, Applicants' claimed invention is directed to a method for producing a semiconductor device having a fluorine-doped silicon oxide layer as well as a silicon oxide layer formed on the fluorine-doped silicon oxide layer.

Advantageously, Applicants have discovered that significant improvements over prior art techniques can be achieved by forming the silicon oxide layer on or above the fluorine-doped silicon oxide layer at a temperature that is at least 10% higher than a film forming temperature of the fluorine-doped silicon oxide layer.

For example, in the first embodiment, the FSG layer 13 is formed at a temperature 380°C and the NSG layer is formed at a temperate of 430°C. Applicants note that the prior art cited by the Examiner, the Jang U.S. Patent No. 6,165,915 is directed to a much different manufacturing process which does not achieve the advantageous benefits and characteristics of the semiconductor products that are manufactured in accordance with Applicants' claimed manufacturing techniques.

More specifically, for example, the Jang reference merely discloses that a fluorosilicate glass layer is first provided on a substrate and thereafter a barrier layer is formed thereon as well as planarized second halogen-doped glass layer. A review of the processing characteristics described by the Jang reference confirms that the temperature ranges for the formation of the fluorosilicate glass layer as well as the barrier layer which may be an undoped silicon glass layer are identical. Consequently, there is simply no teaching or suggestion whatsoever regarding Applicants' claimed manufacturing techniques which rely upon significant temperature differences in the manufacturing temperatures.

Advantageously, as described in Figure 3, the resultant semiconductor product characteristics of products that are manufactured in accordance with Applicants' techniques have far improved qualities over those which were manufactured over prior art techniques including those of the Jang reference. Accordingly, in light of the foregoing, Applicants submit that all claims now stand in condition for allowance.

Furthermore, as an additional point of distinction, Applicants note that claim 4 in the instant application is directed to an alternate embodiment of the present invention wherein the fluorine-doped silicon glass layer is initially formed and a surface layer of the fluorine-doped silicon glass layer is removed by sputtering in a same process chamber subsequent to formation of the fluorine-doped silicon glass layer. There is simply no teaching or suggestion whatsoever regarding this alternate manufacturing technique in the references cited by the Examiner.

Accordingly, at the very least, for this reason alone, Applicants' invention is patentability distinct over the art of record. In light of the foregoing, Applicants respectfully request that the Examiner now withdraw the rejections and allow all claims in the application.

Respectfully submitted,

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(Reg. #37,607)

Robert J. Depke
HOLLAND & KNIGHT LLC
131 South Dearborn Street, 30th Floor
Chicago, Illinois 60603
Tel: 312.422.9050
Fax: 312.578.6666
Attorney for Applicants

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail on May 5, 2003 in an envelope addressed to:

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Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney for Applicants

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